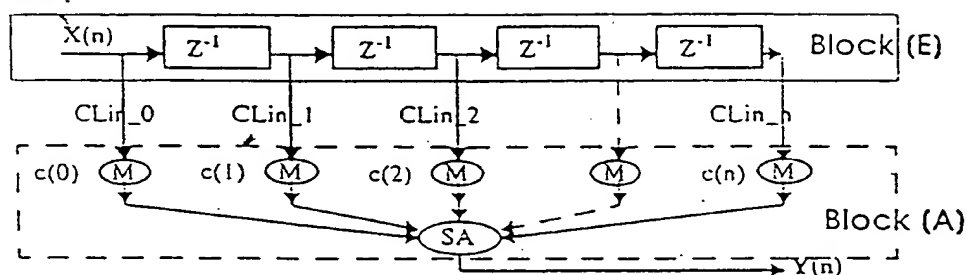
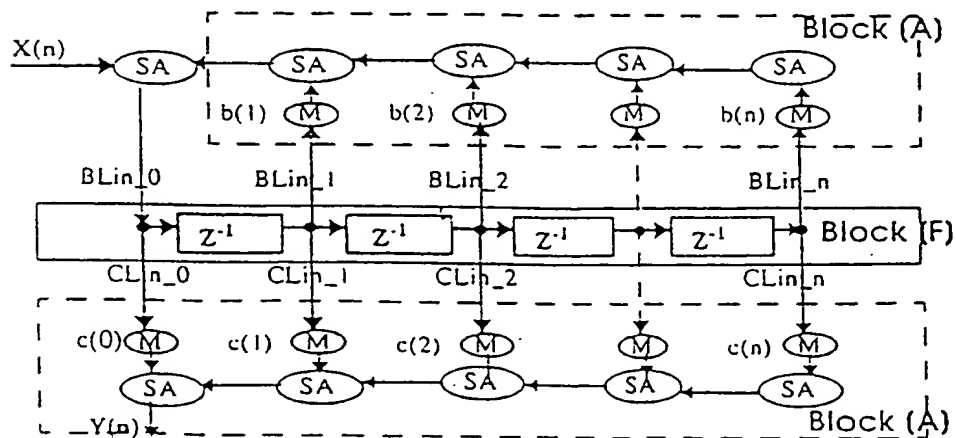
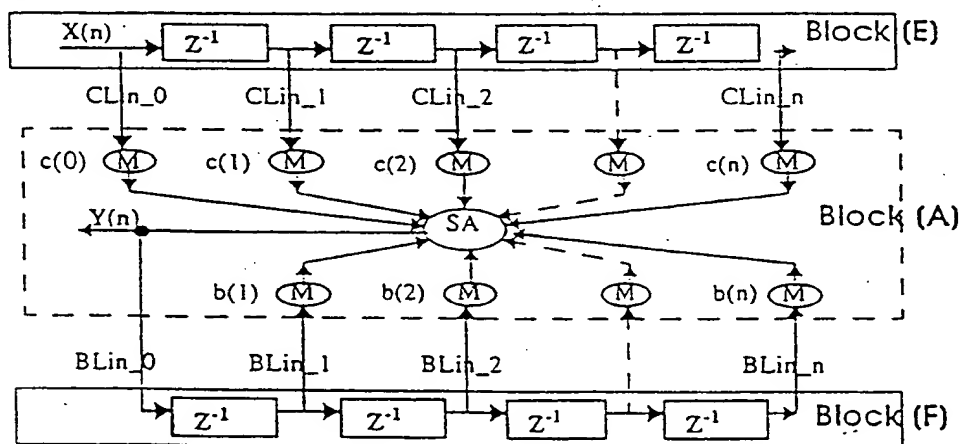
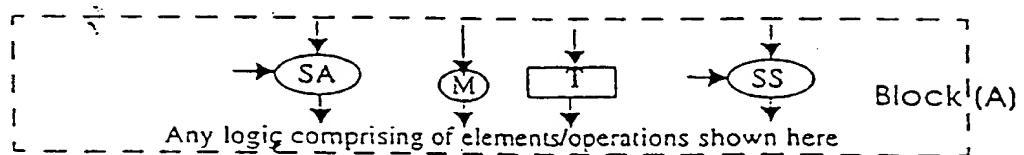


FIGURE 1. Field of invention.

FIR filterIIR filter

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Other Application (Combination, sequential logic minimization)FIR/IIR filter equation

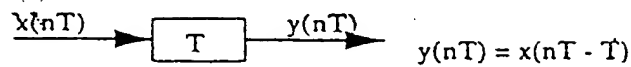
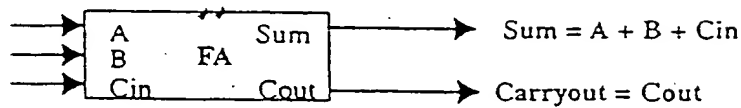
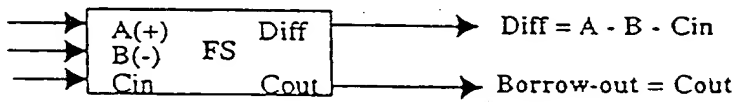
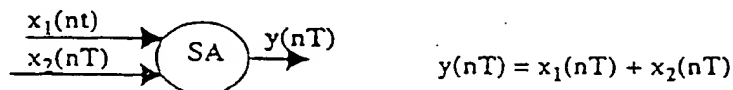
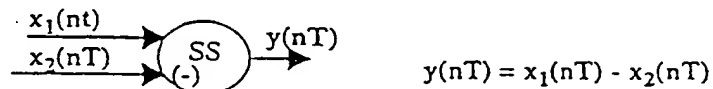
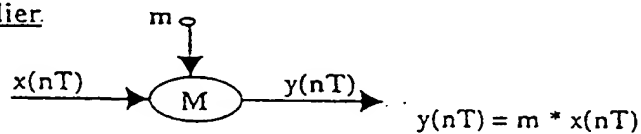
$$Y(z) = X(z) [c(0) + c(1) Z^{-1} + c(2) Z^{-2} + c(3) Z^{-2} + \dots + c(n) Z^{-n}] \quad \dots \text{FIR Eq}$$

$$Y(z) = X(z) \frac{[c(0) + c(1) Z^{-1} + c(2) Z^{-2} + c(3) Z^{-2} + \dots + c(n) Z^{-n}]}{[1 - (b(1) Z^{-1} + b(2) Z^{-2} + b(3) Z^{-2} + \dots + b(m) Z^{-m})]} \quad \dots \text{IIR Eq}$$

where $X(z)$ -input signal, $Z^{-1} * X(z)$ - delayed signal by one delay, $Y(z)$ -output signal
 $c(0), c(1), c(2), \dots, c(n), b(1), b(2), \dots, b(m)$ are integer coefficients values.

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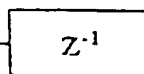
FIGURE 2. Bit Serial Elements/components

Unit DelayFull adderFull subtractorSerial adderSerial subtractorMultiplierDelay

Input Frame size = X bits (e.g input is 1010101 or X=7 bits)

To store X bit frame, number of T element used is X or 7 in present case

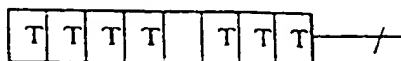
Serial one bit Input
Frame size (X bits)



Serial one bit Output
Frame size (X bits)

Serial one bit Input
Frame size (X bits)

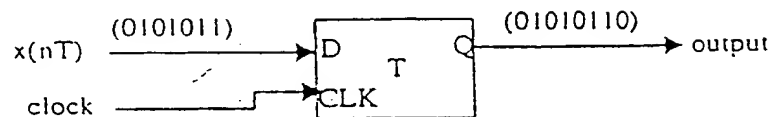
OR



$$\text{Eq } y(n) = x(n-1)$$

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FIGURE 3. Explanation about components used

Unit Delay

Input frame Input pattern (0101011) is coming serially at x(nT) pin at clock rate specified on clock pin

Full adder (FA) / Full subtractor (FS)

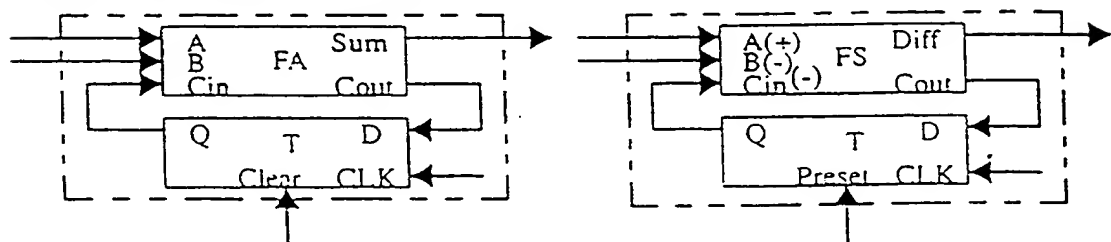
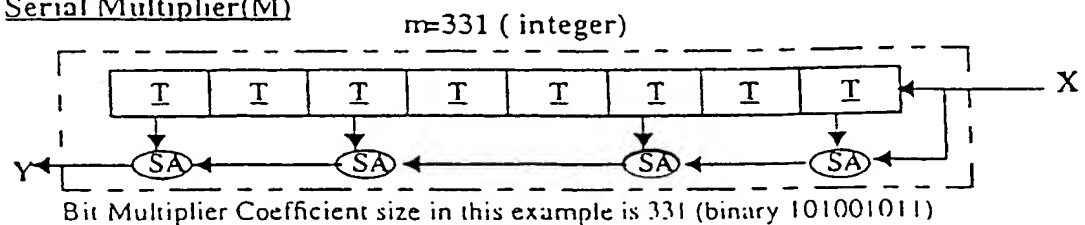
binary addition/subtraction components is realized using following truth table

Truth table - Full adder

A	B	Cin	Z	Co
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

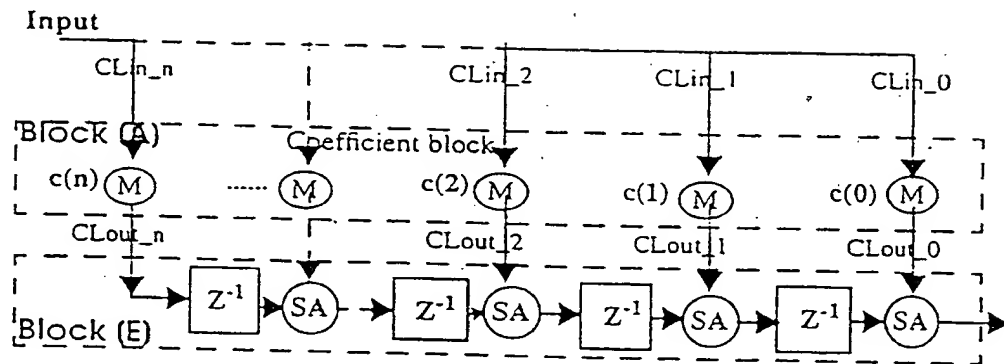
Truth table - Full Subtractor

A	B	Cin	Z	Co
0	0	0	0	0
0	0	1	1	1
0	1	0	1	1
0	1	1	0	1
1	0	0	1	0
1	0	1	0	0
1	1	0	0	0
1	1	1	1	1

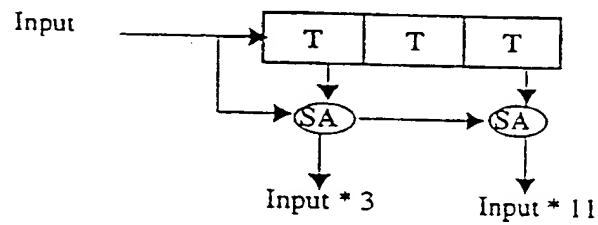
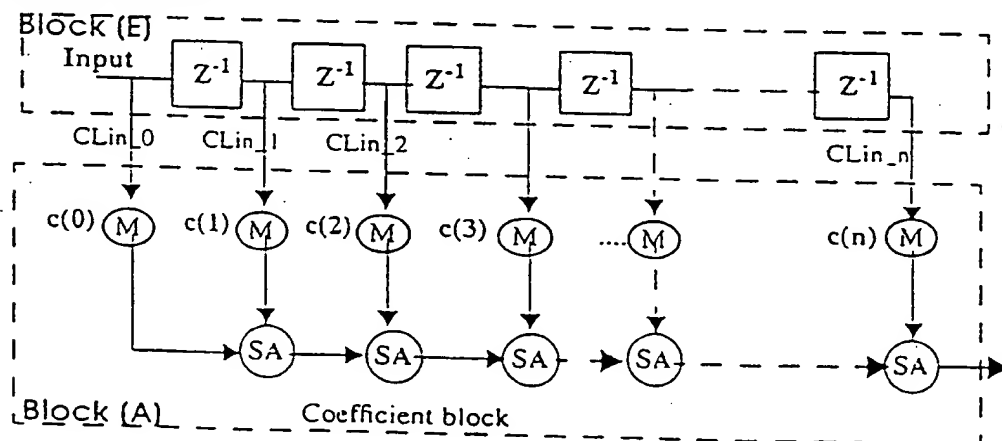
Serial Adder(SA) / Subtractor (SS)Serial Multiplier(M)

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FIGURE 4. Bit Serial Implementation of FIR Filter

Implementation 1

Realization of coefficient using share-able multiplier (coeff. = 3, 11)

Implementation 2

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FIGURE 5. Example FIR Filter

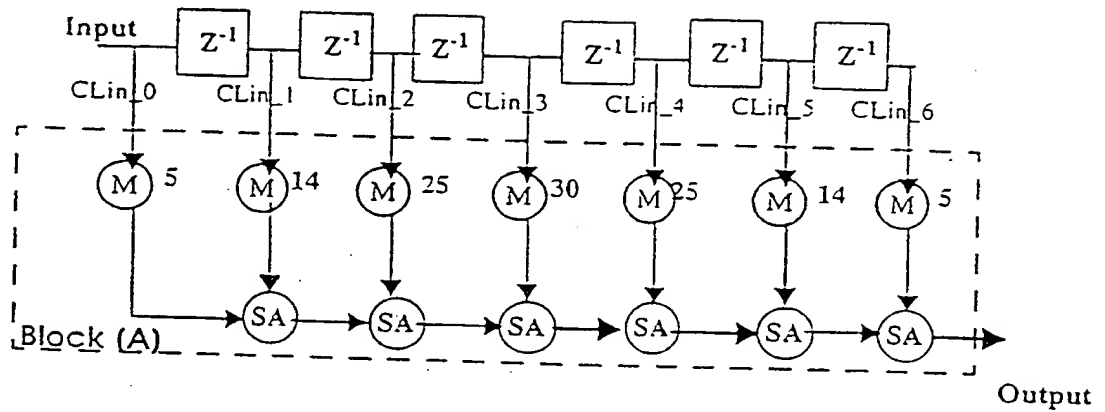
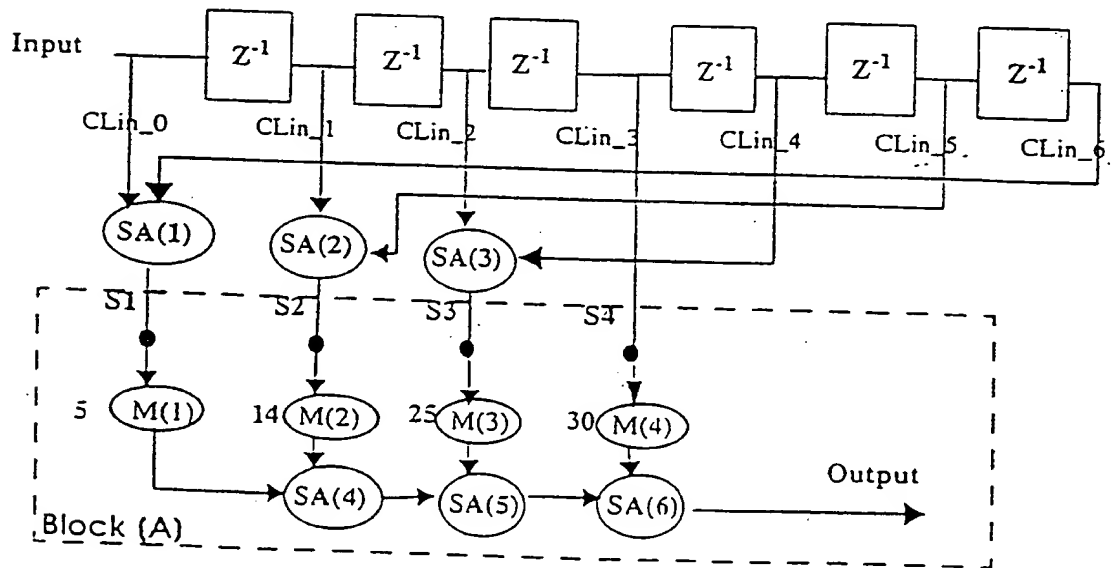


FIGURE 6. An Existing Minimization Technique



Begin: Using the property of symmetrical coefficient

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FIGURE 7. The "Existing Implementation" of the Coefficient Block [A]

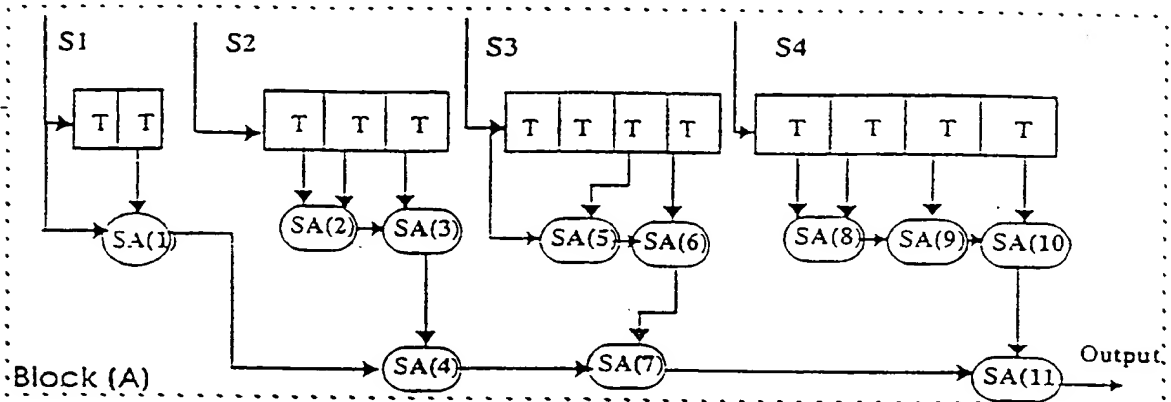
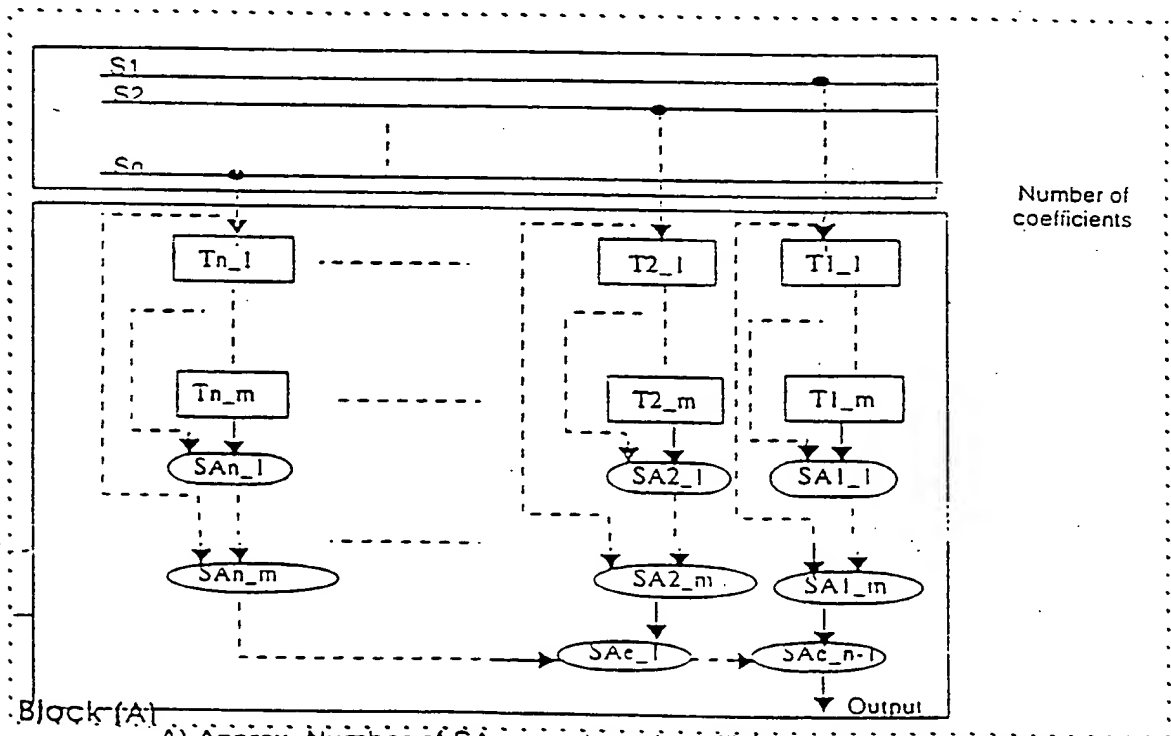


FIGURE 8. Generalized structures for "Existing Methods & minimizations"

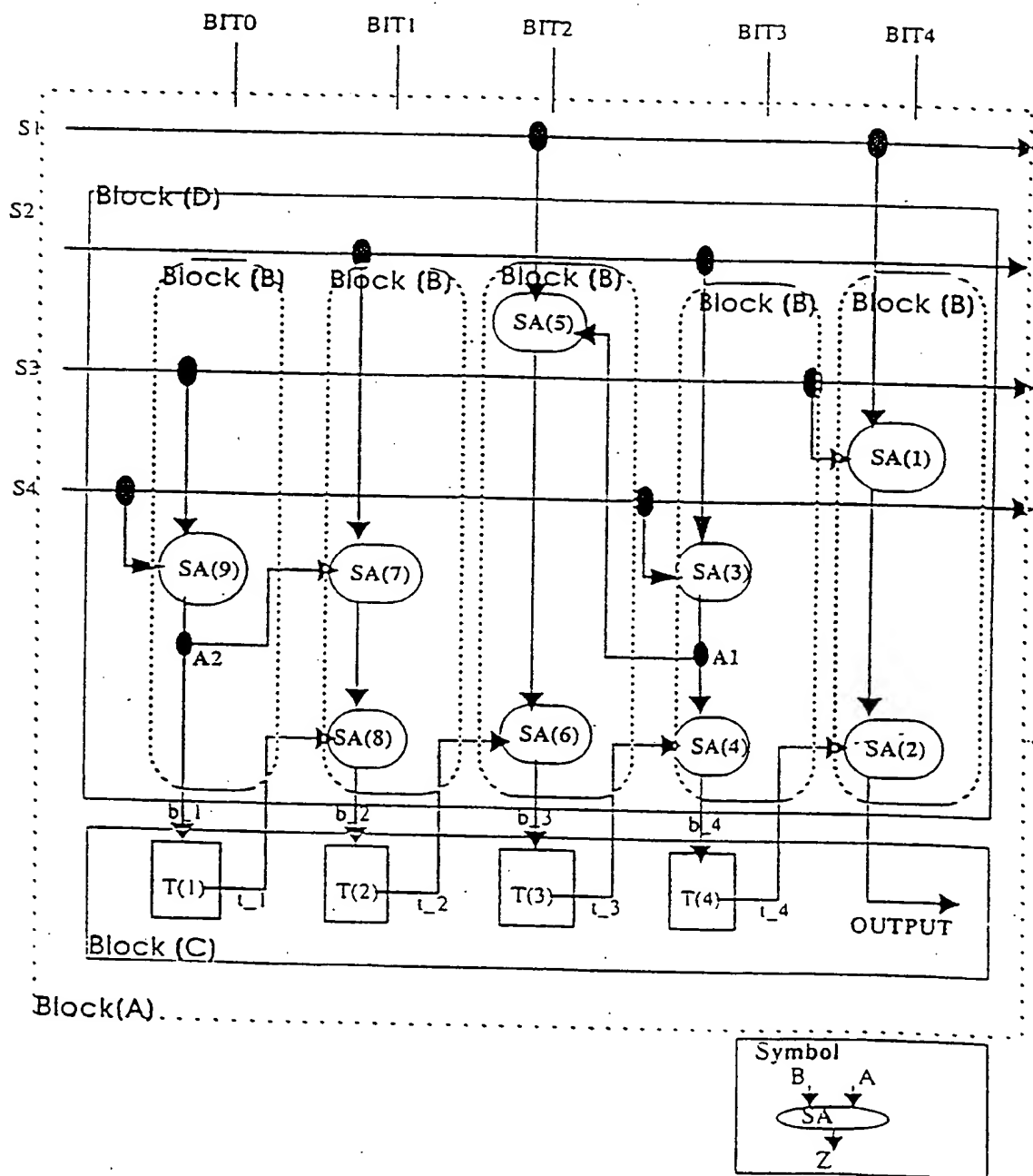


A) Approx. Number of SA = number of coefficient * max coeff size / 2)

B) Flip-flop (T) are not sharable

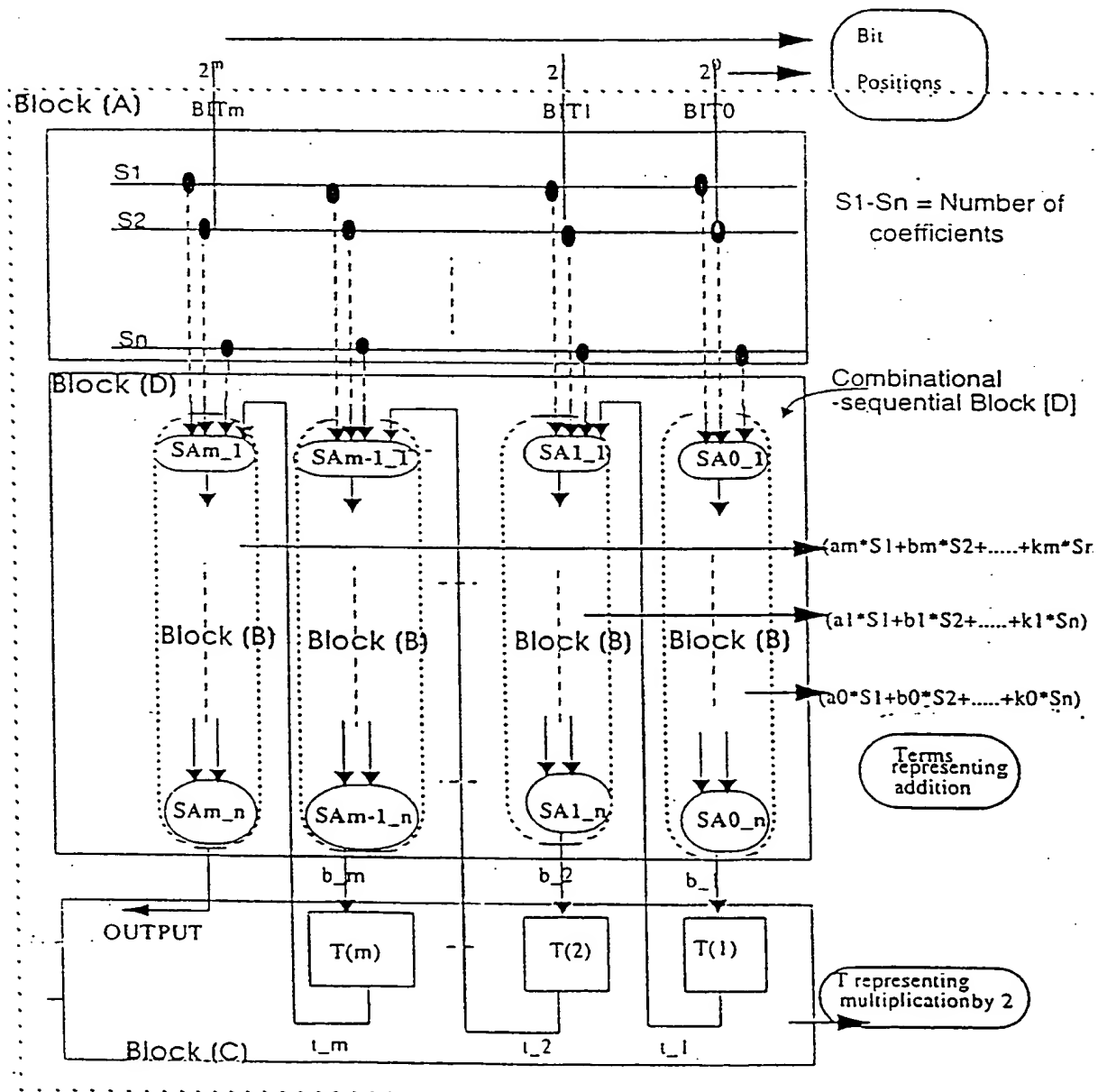
Approx. Number of flip-flops - number of coeff * (max. coefficient size/2)

FIGURE 9. Minimization (Already applied as patent)



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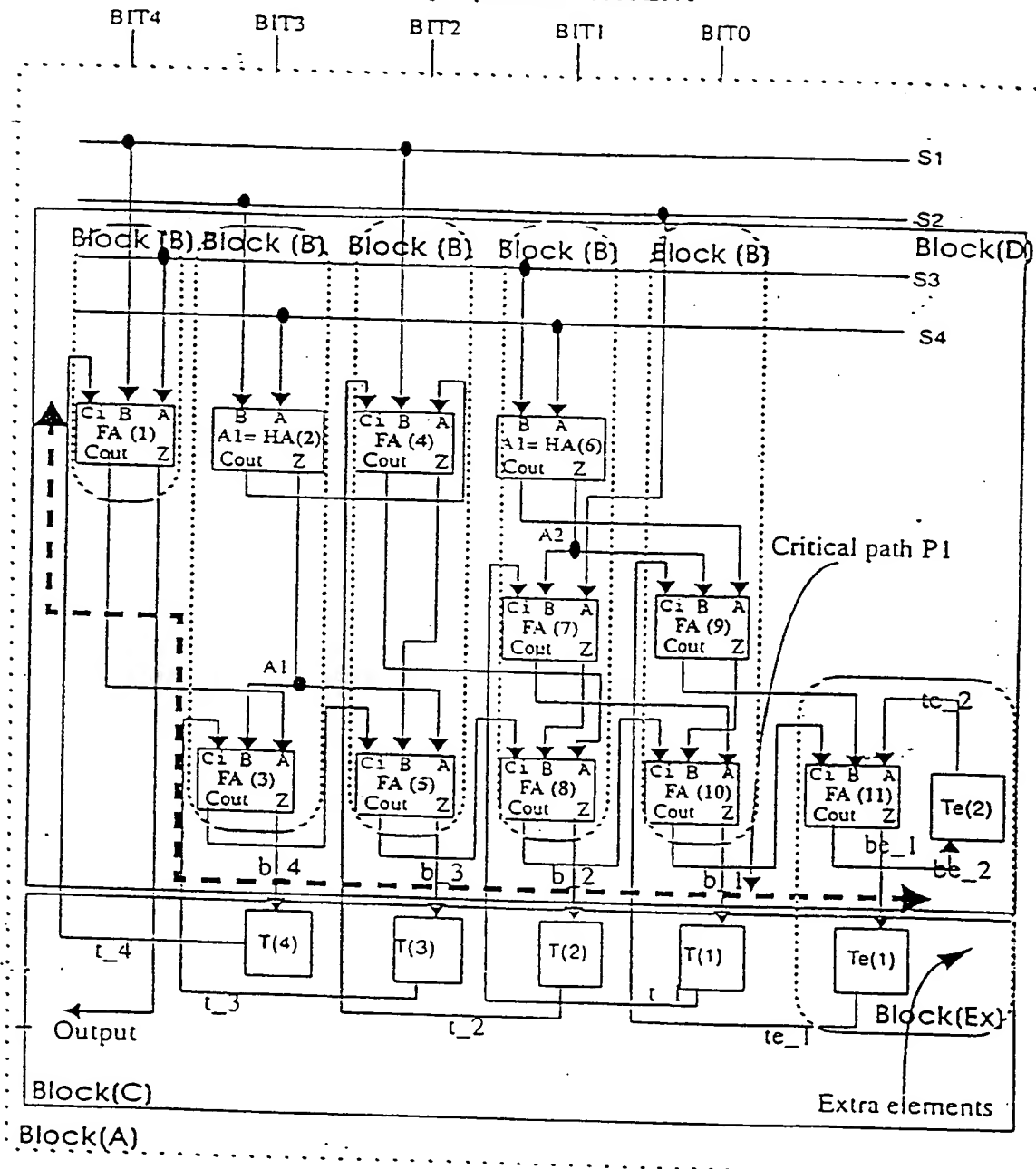
FIGURE 10. Generalized structure "Minimization already applied as patent"



Approx. Number of serial adders = $\frac{\text{number of coefficient}}{\text{max coeff size / 2}}$
 Number of flip-flops(l) = Size of maximum coefficient

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FIGURE 11. Minimizations in "proposal for PATENT"



[illegible]

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FIGURE 13. MSBs of the Parallel output are directly available

